What is claimed is:

1. In a data processing memory assembly of the type having an input port, an output port, and containing information stored in a plurality of addressable storage locations, said memory assembly being responsive in processing to data having an address information portion and a to be stored portion, the improvement comprising said processing including a selective capability of directing said address information portion of said data appearing in a data path to said plurality of addressable storage locations in a separate processing path without disturbing said information stored in said plurality of addressable storage locations.

2. The improvement of claim 1 wherein said selective capability includes a separate address information path around said addressable storage locations to said output port, and, a processing instruction implementing the directing of said address information portion of said data to said separate path.

3. The improvement of claim 2 including a data processing capability responsive to data through said separate path delivered to said output port.

4. The improvement of claim 3 wherein said separate address information path is from an address register in said memory assembly through a serializer to an output buffer in said memory assembly, and said processing instruction is from a timing register through a serializer to said output buffer in said memory assembly.

5. The improvement of claim 2 wherein said processing instruction disables entry of to be stored information into said plurality of addressable storage locations.

6. The improvement of claim 2 wherein said processing instruction employs an unused in a standard storage event condition on a terminal in combination with a burst stop command in said memory assembly.

7. In an addressable random access memory of the type having a plurality of storage locations, being responsive in processing to data increments having an address portion and a to be stored portion, and having a register for direction of specific data increments to specific ones of said plurality of storage locations, the method of verifying that the location in said plurality of storage locations to which a specific increment of said data increments was directed is the location in which it resides,
comprising the steps of:
directing said address information portion of said data, appearing in a data path to said plurality of addressable storage locations, through a separate path around said plurality of addressable storage locations, to an output location,
providing at said output location access in said register to the assigned location in which each data increment was to be stored, and,
comparing the data in said separate path with said register for a difference of storage location.

8. The method of claim 7 wherein said separate path is a path between an address register element and said output buffer element.

9. The method of claim 8 wherein said register for direction of specific data increments to specific ones of said plurality of storage locations is a mode register element, and said output location is an output buffer element.

10. The method of claim 9 wherein a copy of the entries in said mode register element is stored in separate computation apparatus connected to said output buffer element.

11. In an addressable random access memory of the type having a plurality of storage locations, being responsive in processing to data increments having an address portion and a to be stored portion, and having a register for direction of specific data increments to specific ones of said plurality of storage locations, the method of tuning the timing of said random access memory assembly for optimization of said address portion of a data increment and the clock function of said memory,

comprising the steps of:

directing said address information portion of said data, appearing in a data path to said plurality of addressable storage locations, through a separate path around said plurality of addressable storage locations, to an output location,

providing at said output location separately stored increments said clock function and separately stored address portions of said data, and,

comparing the data in said separately stored address portions of said data with a corresponding pulse from said clock function and identifying events where said clock function pulse occurred other than during said address portion of said data.path with said register for a difference of storage location.

12. The method of claim 11 including the step of adjusting the output of said clock function to position said corresponding pulse to the center of the duration of said address portion of said data.

13. In an addressable random access memory having a plurality of data array banks arranged in columns and rows, having provision for read and write signals to said banks in separate command cycles multiplexed into a common data bus under control of the control and decoding circuitry of said columns and having power driving elements for each of said banks,

the improvement for calibration of the impedance of said driver elements comprising:

means for providing, during a write command cycle, an adjust signal operable to disable input from

said common data bus into said array bank, and to disconnect said write command signal from the circuitry of said columns,

means for delivering impedance control vector signals, indicating at least one of change of magnitude and of satisfaction with the present impedance state, to each of said power driving elements, and,

means for producing impedance control instructions on said common data bus, said instructions being operable to select from tabulated values of said at least one of change of magnitude and of satisfaction with the present impedance state, and delivering said instructions to said impedance control vector delivery means.

14. The method of calibrating the impedance of power driving elements that drive read and write operations in an addressable random access memory having a plurality of data array banks arranged in columns and rows, having provision for read and write signals to said banks in separate command cycles multiplexed into a common data bus under control of the control and deecoding circuitry of said columns and having power driving elements for each of said banks,

comprising the steps of:

providing, during a write command cycle, an adjust signal, operable to disable input from said common data bus into said array bank, and to disconnect said write command signal from the circuitry of said columns,

delivering impedance control vector signals, indicating at least one of change of magnitude and of satisfaction with the present impedance state, to each of said power driving elements,

producing impedance control instructions on said common data bus, said instructions being operable to select from tabulated values of said at least one of change of magnitude and of satisfaction with the present impedance state, and,

delivering said instructions to said each of said power driving elements.

15. In an addressable random access memory having a plurality of data array banks arranged in columns and rows, having provision for read and write signals to said banks in separate command cycles multiplexed into a common data bus and having power driving elements for each of said banks, the improvement for calibration of the impedance of said driver elements comprising:
means for providing, during a write command cycle, adjust up and adjust down signals operable to provide clocked latched and decoded input to each said driver element as impedance control vector signals, indicating at least one of change of magnitude and of satisfaction with the present impedance state, to each of said power driving elements.

16. In an addressable random access memory having a plurality of data array banks arranged in columns and rows, having provision for read and write signals in separate cycles to said banks multiplexed into a common data bus and having power driving elements for each of said banks,
the improvement for adjustment of timing skew in operation of said memory comprising:
means for placing into said common data bus, in one said read cycle, during the duration of a column access time, a uniform set of serial signals, and,
means for holding enablement of delivery of said uniform set of serial signals until the start of access of a column.

17. The improvement of claim 16 including an align signal operable to disconnect data array banks from said common data bus.

18. In an addressable random access memory assembly,

said assembly having an input port and an output port,

said assembly having a plurality of drivers, driving, through a common communication channel data path, data array banks arranged in columns and rows,

the improvement comprising:

means providing separate read and write cycles, and,

means ,taking place during a said read cycle, for redirection of address data, from a said data path to said data array banks, to a data path to at least said output port.

19.The improvement of claim 18 wherein during said read cycle said address data is received through a column decoder.

20. The improvement of claim 19 wherein during said read cycle said address data is held until the beginning of the address.